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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,852	07/16/2003	Yanjun Ma	SLA0815 (SMT324D)	1808

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/621,852	MA ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 7, 2004 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kittl et al. (US 2002/0045307A1) in view of Chapman (US Pat. No. 6,010,929).

Regarding claims 16, 18 and 20, Kittl et al. teaches a sub-micron MOS transistor comprising: a substrate (400); and

an active region (portion of the substrate (400) in which source/drain regions, LDD regions, and channel region are formed) including:

a gate region (portion of the substrate beneath the gate (408) and located between the regions (410). See fig. 4b) having a length of less than one micron (see paragraph [0038] and Fig. 4b). [1]

a. source region (412) including a LDD source region (410) (see fig. 4c); and

a drain region (412) including a LDD drain region (410) (see fig. 4c).

With regards to claim 20, Kittl teaches a gate oxide layer (402) overlying the gate region (portion of the substrate located between regions 410 and beneath gate 408) having a length about twice as long as the gate region length (please noted that the length of the gate oxide 402 appears to be about twice as long as the length of the region of the substrate located between regions 410 and beneath gate 408. See fig. 4b and 4c).

However, Kittl et al. fails to teach the ion concentration of said source region and said drain region of between about 1 x 10^{20} cm^{-3} to 1x 10^{21} cm^{-3}, and the ion

[1] In paragraph [0038], last sentence, Kittl et al. teaches a gate length of less than 0.1 microns; and in Figure 4b teaches a gate region having the same length as the gate (408).

concentration of said LDD source region and said LDD drain region of between about 1 x 10^{19} cm^{-3} to 5 x 10^{19} cm^{-3}.

Chapman teaches that it is well known in the art to form the source and drain regions having an ion concentration of between about 10^{20} cm^{-3} (col. 4, lines 50 and 52), and LDD regions having an ion concentration of between about 10^{19} cm^{-3} (col. 4, lines 3-4).

Kittl et al. and Chapman are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include source and drain regions having an ion concentration of between about 10^{20} cm^{-3} (col. 4, lines 50 and 52), and LDD regions having an ion concentration of between about 10^{19} cm^{-3}. The motivation for doing so, is reducing short channel effects. Therefore, it would have been obvious to combine Chapman with Kittl et al. to obtain the invention of claims 16-21.

Regarding claims 17 and 19, Kittl et al. teaches an insulating oxide (402) (see fig. 4c), source and drain electrode contact (426) and gate electrode contact (428) (see fig. 4f).

Regarding claim 21, Kittl et al. teaches an insulating oxide (402) (see fig. 4c), source and drain electrode contact (426) and gate electrode contact (428) (see fig. 4f), wherein the gate electrode contact has a length of about half the length of the gate oxide layer (see fig. 4f) [2].

[2] Figure 4f shows a gate oxide (422) having a length which is longer than the length of the gate electrode contact (428). To determine the length of each layers, the examiner measured the length of the gate electrode contact and the gate oxide by using a conventional ruler. The examiner found that the gate oxide is about 3.7 cm long and the gate electrode contact is about 2.4 cm long, which is 65% of the length

Response to Arguments

5. Applicant's arguments with respect to claims 16-21 have been considered but are moot in view of the new ground of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ozaki (Us Pat. No. 5,159,417) discloses in figure 9 a transistor having a gate oxide (3), source and drain regions (51, 61) having a concentration of 10^{21} cm^{-3} (col. 9, lines 53-54), and LDD regions (50, 60) having a concentration of 10^{19} cm^{-3} (col. 9, lines 19-20).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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of the gate oxide. Please note that the examiner interpreted the limitation "about half" as a broad range that includes values higher than 50% but less than 75%.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

4/26/05

José R. Díaz
Examiner
Art Unit 2815